

IPD49CN10N G-VB Datasheet

N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.030 at $V_{GS} = 10$ V	40
	0.035 at $V_{GS} = 4.5$ V	37

FEATURES

- Trench Power MOSFETS
- 175 °C Junction Temperature
- Low Thermal Resistance Package



Available
RoHS*
 COMPLIANT



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	40	A
		23	
Pulsed Drain Current	I_{DM}	120	
Avalanche Current	I_{AR}	35	
Repetitive Avalanche Energy ^a	E_{AR}	61	mJ
Maximum Power Dissipation ^a	P_D	107 ^b	W
		3.75	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	1.4	

Notes:

a. Duty cycle ≤ 1 %.

b. See SOA curve for voltage derating.

c. When Mounted on 1" square PCB (FR-4 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{SS} = 0 V, I _D = 250 μA	100			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	75			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 5 A		0.030		Ω
		V _{GS} = 4.5 V, I _D = 3 A		0.035		
		V _{GS} = 10 V, I _D = 5 A, T _J = 125 °C		0.053		
		V _{GS} = 10 V, I _D = 3 A, T _J = 175 °C		0.067		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 15 A	10			S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		2600		pF
Output Capacitance	C _{oss}			290		
Reverse Transfer Capacitance	C _{rss}			120		
Total Gate Charge ^c	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 40 A		35	60	nC
Gate-Source Charge ^c	Q _{gs}			11		
Gate-Drain Charge ^c	Q _{gd}			9		
Gate Resistance	R _G			1.7		Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 50 V, R _L = 1.25 Ω I _D ≅ 40 A, V _{GEN} = 10 V, R _G = 2.5 Ω		11	20	ns
Rise Time ^c	t _r			12	20	
Turn-Off Delay Time ^c	t _{d(off)}			30	45	
Fall Time ^c	t _f			12	20	
Source-Drain Diode Ratings and Characteristics T _C = 25 °C ^b						
Continuous Current	I _S				40	A
Pulsed Current	I _{SM}				120	
Forward Voltage ^a	V _{SD}	I _F = 30 A, V _{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 30 A, di/dt = 100 A/μs		60	100	ns
Peak Reverse Recovery Current	I _{RM(REC)}			5	8	A
Reverse Recovery Charge	Q _{rr}				0.15	0.4

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Output Characteristics



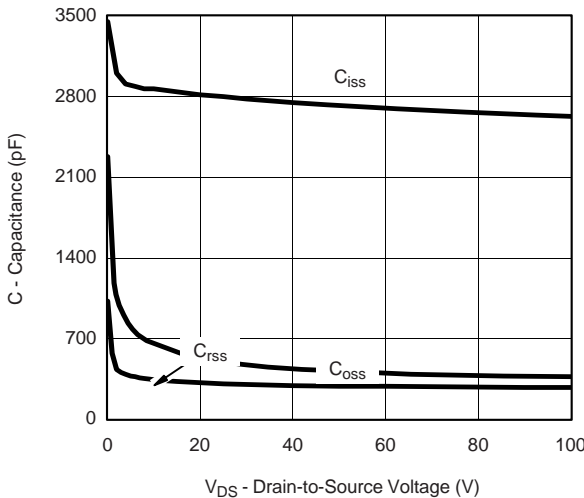
Transfer Characteristics



Transconductance



On-Resistance vs. Drain Current



Capacitance



Gate Charge

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



Avalanche Current vs. Time



Drain-Source Breakdown Voltage vs. Junction Temperature

THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

TO-252AA CASE OUTLINE



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12				
DWG: 5347				

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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